ABSTRACT OF THE DISCLOSURE

In the testing device of a semiconductor integrated circuit, each of the logics is provided with the JTAG circuit includes: a boundary scan register that executes a test of the logic in accordance with a test data input and stores a test result, a data register, a pseudo bypass register having a bypassing function of the test data input, a first selector connected to the data register and the pseudo bypass register, which selectively takes out outputs of the registers, a bypass register having the bypassing function of the test data input, an instruction register for giving an operation command, and a second selector connected to the boundary scan register, the first selector, the bypass register, and the instruction register, which is selectively controlled by the instruction register. In this construction, the output from the second selector of a specific logic is connected to the input of another logic.